nBand Communications

Fusion
A Unified Communications Processor Platform

8/23/99

nBand Company Profile

- Mission
  - To be a leading digital silicon solutions provider to comm markets for those applications that exhibit significant data level parallelism
- Fabless semiconductor company
  - Initial target market => Wireless infrastructure
    - Multi-mode (2G/2.5G/3G) cellular base station modems
    - Broadband wireless modems
  - Related markets
    - Smart (2.5G/3G) cellular phones/communicators/PDAs
- IP licensing component
  - License core to systems partners in other markets
    - Gateways/Access Products
    - xDSL/DSLAM
    - Cable Modem

nBand Strategy

- Target high growth wireless market with **deliverable** technology
  - Proven MIPS RISC processor
  - Vector DSP technology (instead of VLIW or reconfigurable)
- Solve key market needs:
  - Software productivity
    - Single instruction stream uniprocessor approach
  - DSP MIPS for communications channel, UI, multi-media
  - Preserve code investment with binary compatible scalability

nBand Strategy (cont’d)

- SOC platform approach
  - Industry standard MIPS RISC processor, Scalable DSP, and Palmchip CoreFrame peripheral bus
  - Allows rapid development of application specific products
- Binary compatible scalable DSP and embedded DRAM
  - Allows products that **span both low power high integration and high performance domains**
  - Create possibility of **leveraging same hardware platform and software for both ends of the local loop and wireless channel** - creates compelling business proposition
    - Different versions of the same binary code compatible Fusion core

Market Opportunity

The Move to Wireless Data

- 1G - analog voice
- 2G - digital voice, limited data (~9.6 Kbps)
- 3G
  - High bandwidth data (up to 2Mbps)
  - Multi-media capabilities (QOS)
  - Multi-modal and backwards compatible
  - Circuit switched => Packet based
    => **Wireless devices will become internet leaf nodes**
  - Service focus => Location based services/Java
  - **>10x implementation complexity of 2G!**

Harmonization via mult-mode radios
=> PUSH TO SOFT RADIOS!

Market Opportunities (cont'd)

- Convergence products - software integration of multiple communications standards
  - Opportunity for consumer/SOHO products that mix multiple standards in a single chip, software solution:
    - xDSL, HomeRF, Bluetooth, HPNA II
- Spanning both ends of the comm channel
  - Wireless: Base Station/Handset
  - Local Loop: CO DSLAM/subscriber modem

Role of DSPs in 3G

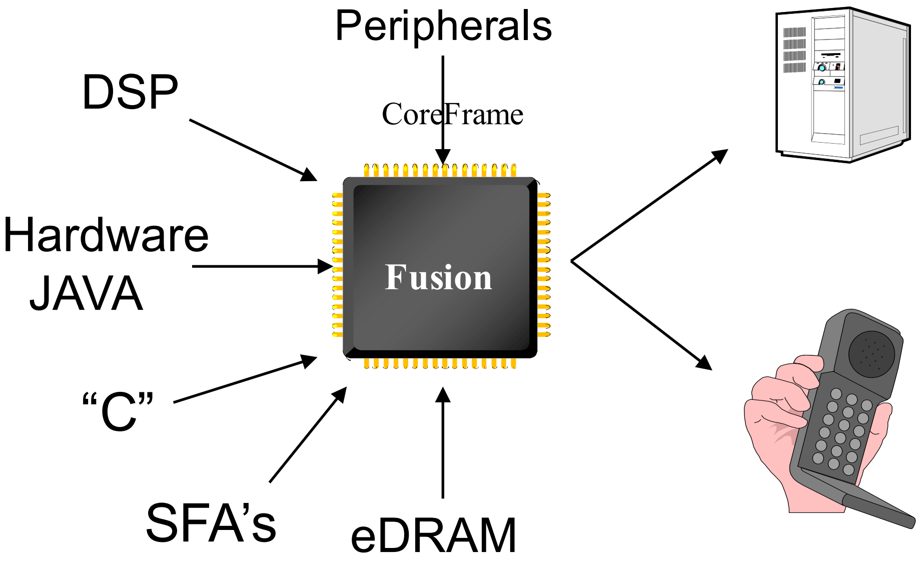
- The role of DSP in 3G cellular will be HUGE!
  - 3G/W-CDMA (intercell asyncronous operation, etc.)
  - Multiple air-interfaces & backwards compatibility
  - Adaptive antennas
  - Space-time coding
  - Multi-user detection & interference cancellation
  - Network management
  - VOIP transcoding

  => adding value/differentiation computationally
- Like 3D graphics, 3G base stations can potentially consume nearly infinite DSP MIPS.

nBand Technology

- Unified hardware architecture (vector DSP + MIPS II microcontroller + hardware JAVA + Embedded DRAM) provides high performance and silicon efficiency.
- Single instruction stream uniprocessor model is leveraged to provide unified software development environment for lower software development $ and time to market. Scalable platform approach preserves code investment.
- Vector DSP architecture leveraged to effectively utilize eDRAM
- Vector approach optimal from a power standpoint for applications exhibiting high data level parallelism
- Efficient embedded hardware Java implementation for Applet execution (value added services) and network management

nBand Communications Processor Platform



- Unified HW and SW architecture
  - 3-in-1 processor
- High performance *vector* DSP
- High MIPS/W
- Hardware JAVA interpreter
- Scalable architecture
- Systems approach
  - Higher integration
  - Embedded DRAM
  - Optimal partitioning
  - Special Function Accelerators

nBand FUSION Capabilities*

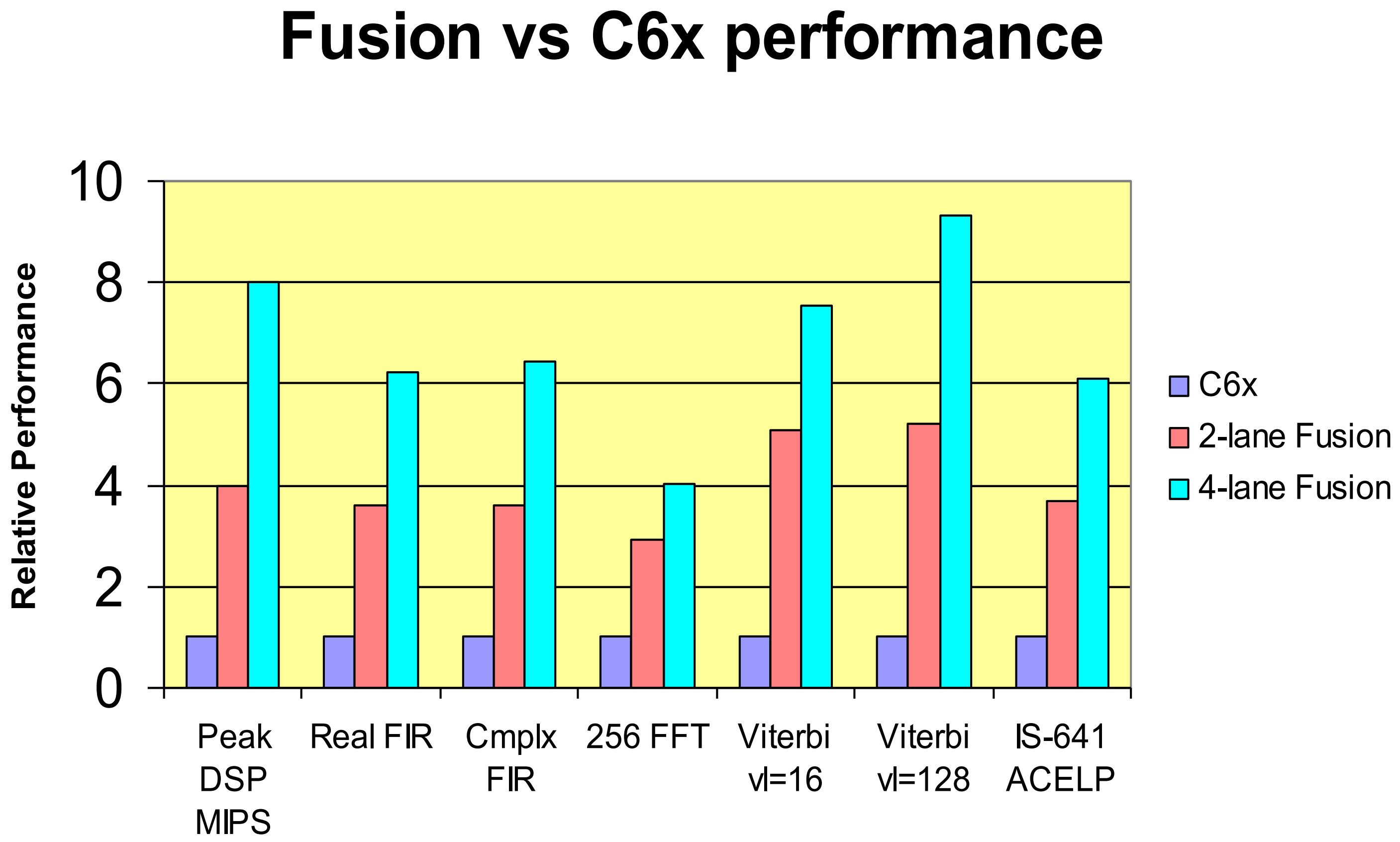
- Executes MIPS-II instructions/binaries
- DSP performance ~6X of TI's C6x at same frequency
  - 3200 DSP MIPS (DSP MIP = 1 Million 16x16 MACs)
- ~4x cellphone DSP MIPS for same power (2-lane system)
- Base station
  - 170-210 enhanced full-rate GSM channels, 20 IS-95 users, **4-5 WCDMA users**
    Java speed 10x conventional interpreter
- Wired applications
  - 10 full CO side, or 4 full client side ANSI DMT ADSL modems
  - single chip (MCU + data pump) cable/satellite modem solutions
  - 24 VOIP channels (G.723) (complete T1)

* Nominal 4-lane 200Mhz std. cell implementation

Algorithms Analyzed

- CDMA - Conv Enc, Viterbi dec, FIR, PN Seq, RS Codec
- ADSL - FFT, RS Codec, Trellis decoder
- VOIP - G.723 Speech codec, FIR
- ACELP Speech Codec - FIR, Min. energy search
- Speech Recognition - FFT, Dynamic Programming
- Encryption - MD5, RSA, DSS, IDEA
- Header Processing - CRC
- JAVA - ExecuteJava.c, javac, ejits, gc, synchronization

Performance Comparison



Business Value Proposition

- Superior price/performance vs other programmable solns
  - Deliverable technology vs alternatives such as reconfigurable
- Lower software development & deployment costs
  - Single instruction stream uniprocessor programming model
- Binary compatible scalability! Supports multi-generational multi-technology platform:
  - Scalable vector DSP (1x - 8x SIMD)
  - Scalable MIPS processor (cache sizes, move to limited dual issue)
  - Scalable Java translator
- Ability to process higher protocol layers
  - Supports standard RTOS
  - Integral MIPS-II compatible microcontroller functionality

Business Value Proposition (cont'd)

- WCDMA => single chip 4-user WCDMA soft radio
  - single chip replaces 4 TI C6x + 4 ASICs
- CDMA
  - single chip replaces 4-5 4-channel Cell Site Modems
- GSM
  - ~15x performance of existing TI C54x implementations
- Access Products
  - Low cost, upgradable, multi-standard, single chip, software based access/gateways

Scalability Options

(binary code compatible)

SuperPipeline
Vector Unit

Add more
vector lanes

Increase eDRAM
Banking

Go SuperScalar

New SFA’s

Not a one trick pony!

Exploiting Scalability

Leverage common hardware and software

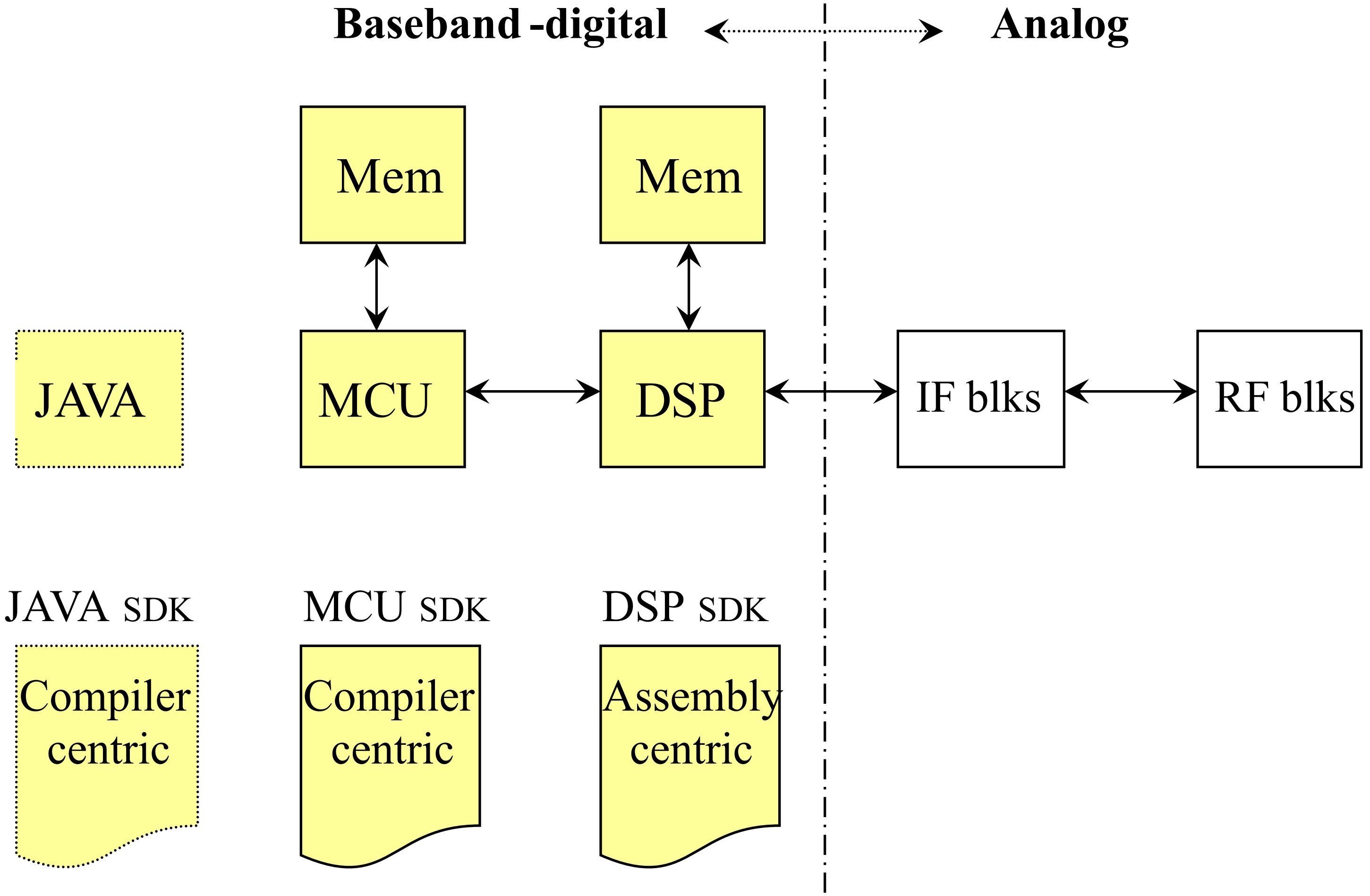
Portable Product ↔ Wireless Channel 2.5G/3G ↔ **Base Station**

Portable Product	Base Station
1-2 lane	4-8 lane
40 Mhz	250 Mhz
1.5-1.8V	1.8-2.5V
2-4 MB eDRAM	2-8MB eDRAM
PCMCIA,USB,Flat Panel,IrDA	cPCI

Subscriber ↔ Local Loop (xDSL) ↔ **CO**

Subscriber	CO
1-2 lane	4-8 lane
200 Mhz	250 Mhz
1.8-2.5V	1.8-2.5V
2-4 MB eDRAM	2-8MB eDRAM
	cPCI

Current Baseband Processor Design



Baseband -digital

Analog

Mem

Mem

JAVA

MCU

DSP

IF blks

RF blks

JAVA SDK

MCU SDK

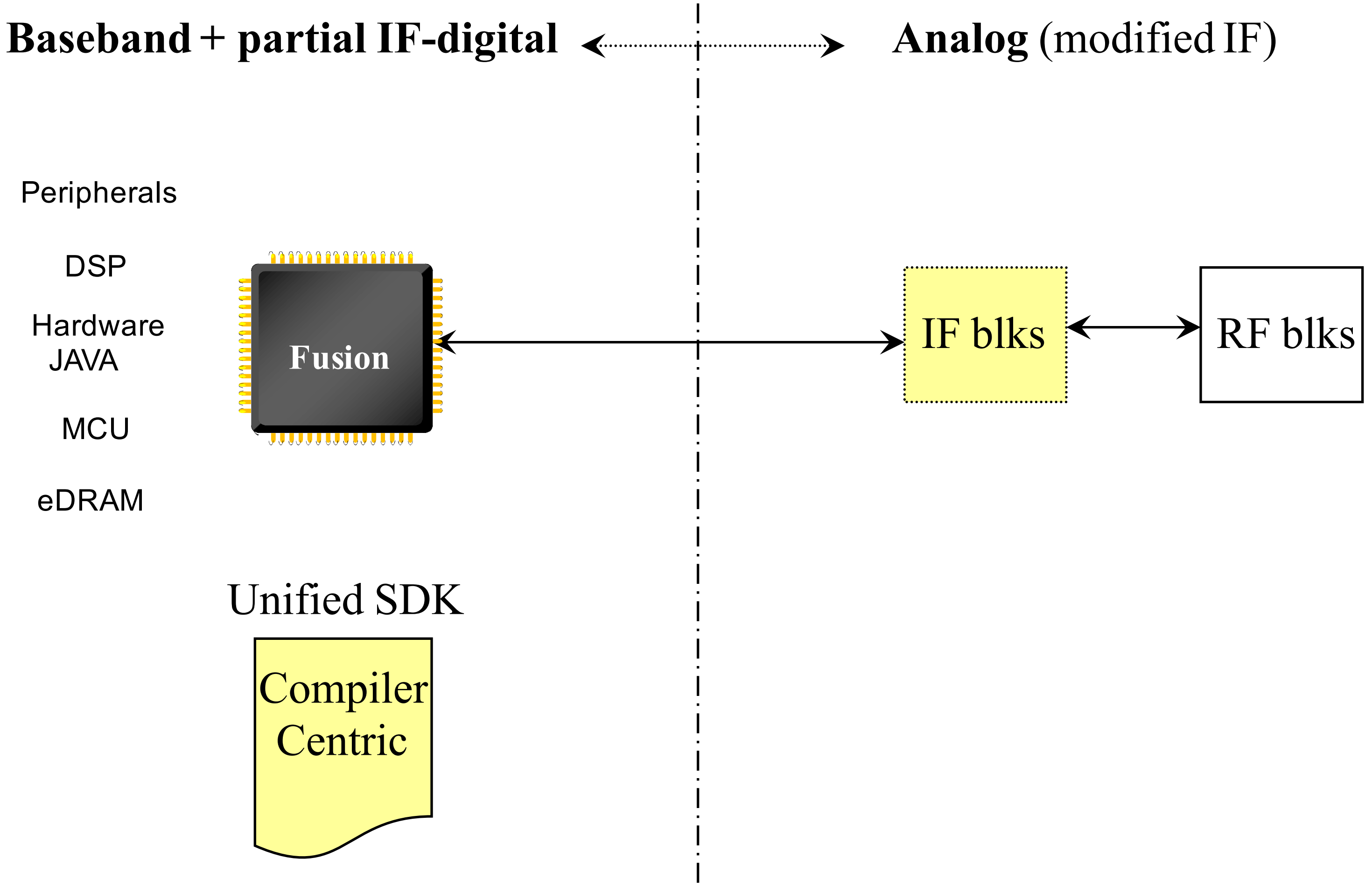
DSP SDK

Compiler centric

Compiler centric

Assembly centric

nBand Solution



Baseband + partial IF-digital ↔ **Analog** (modified IF)

Peripherals

DSP

Hardware
JAVA

MCU

eDRAM

Fusion

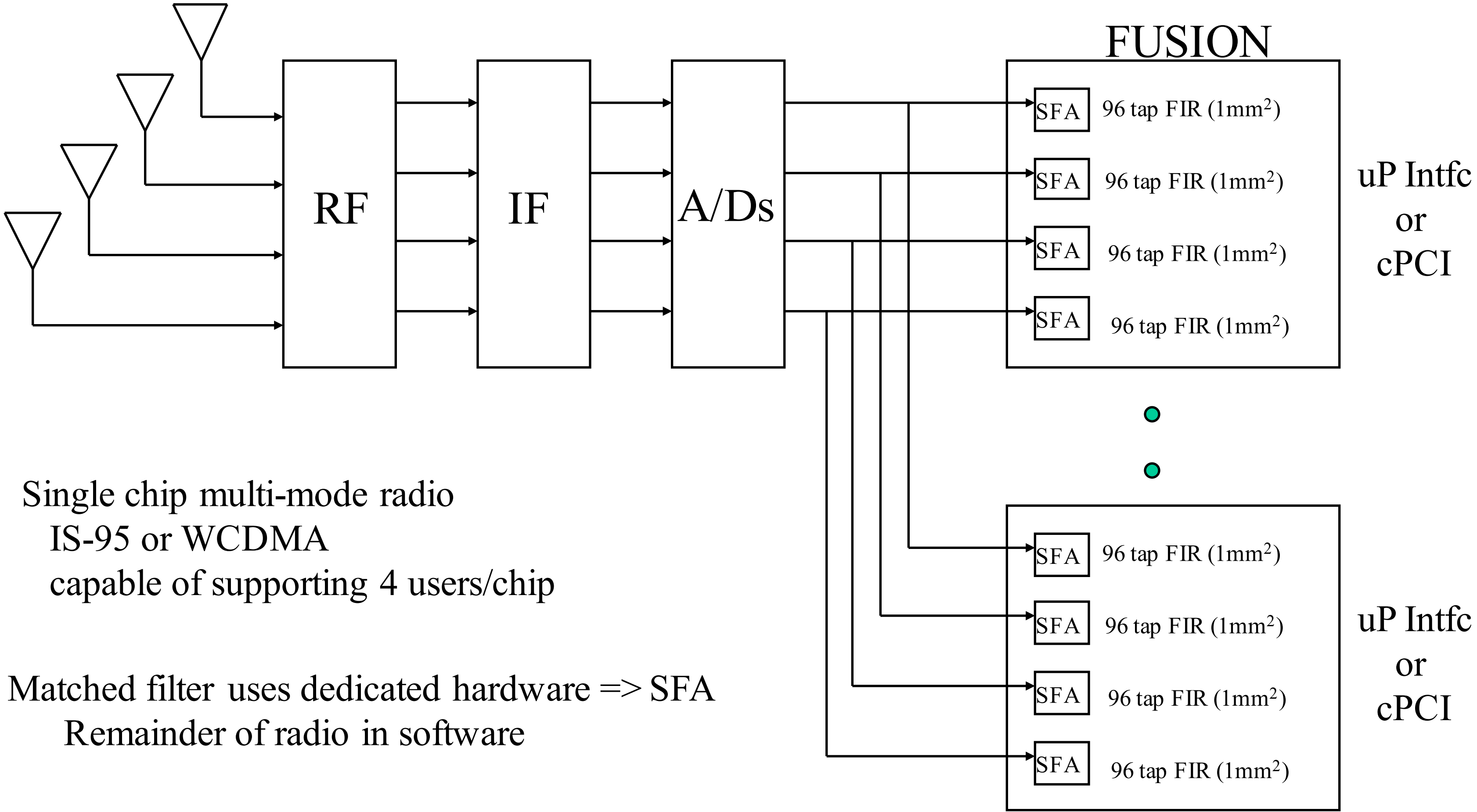
IF blks

RF blks

Unified SDK

Compiler
Centric

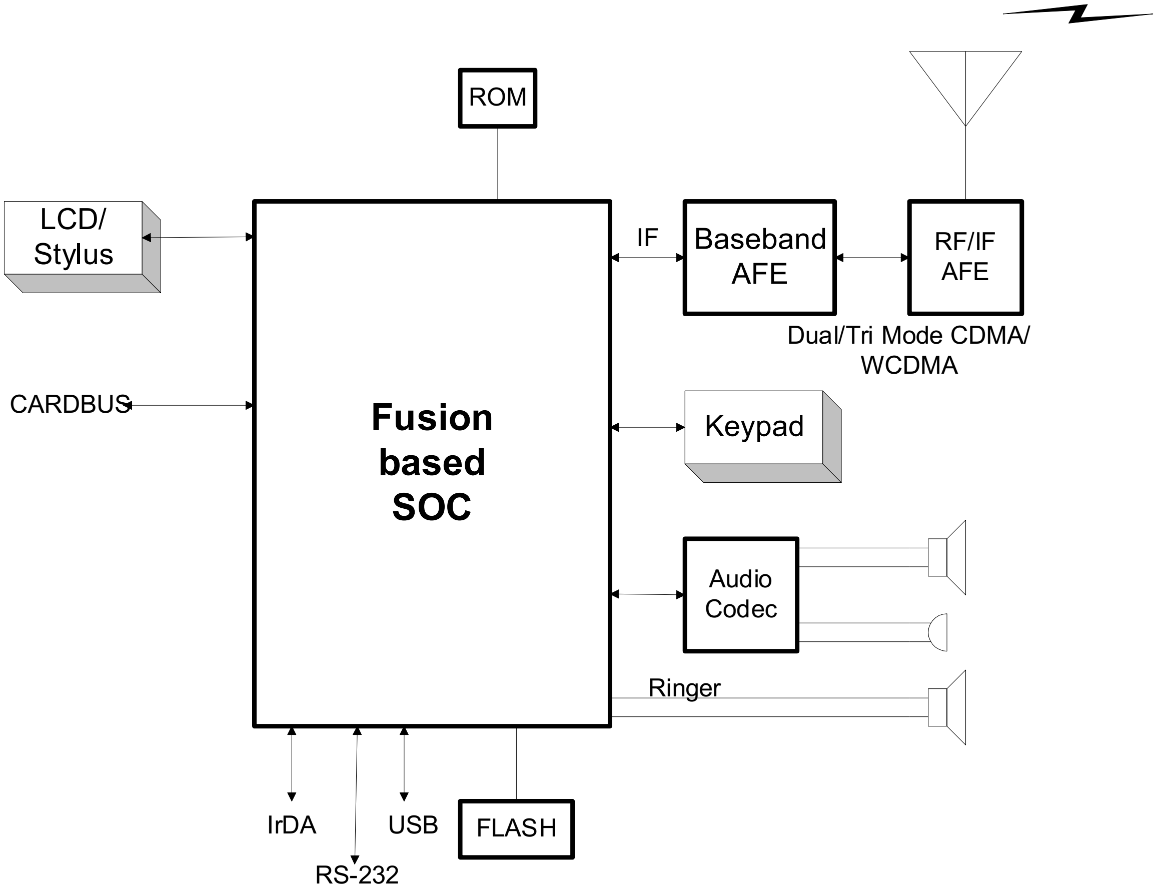
Example WCDMA BS Implementation



Single chip multi-mode radio
IS-95 or WCDMA
capable of supporting 4 users/chip

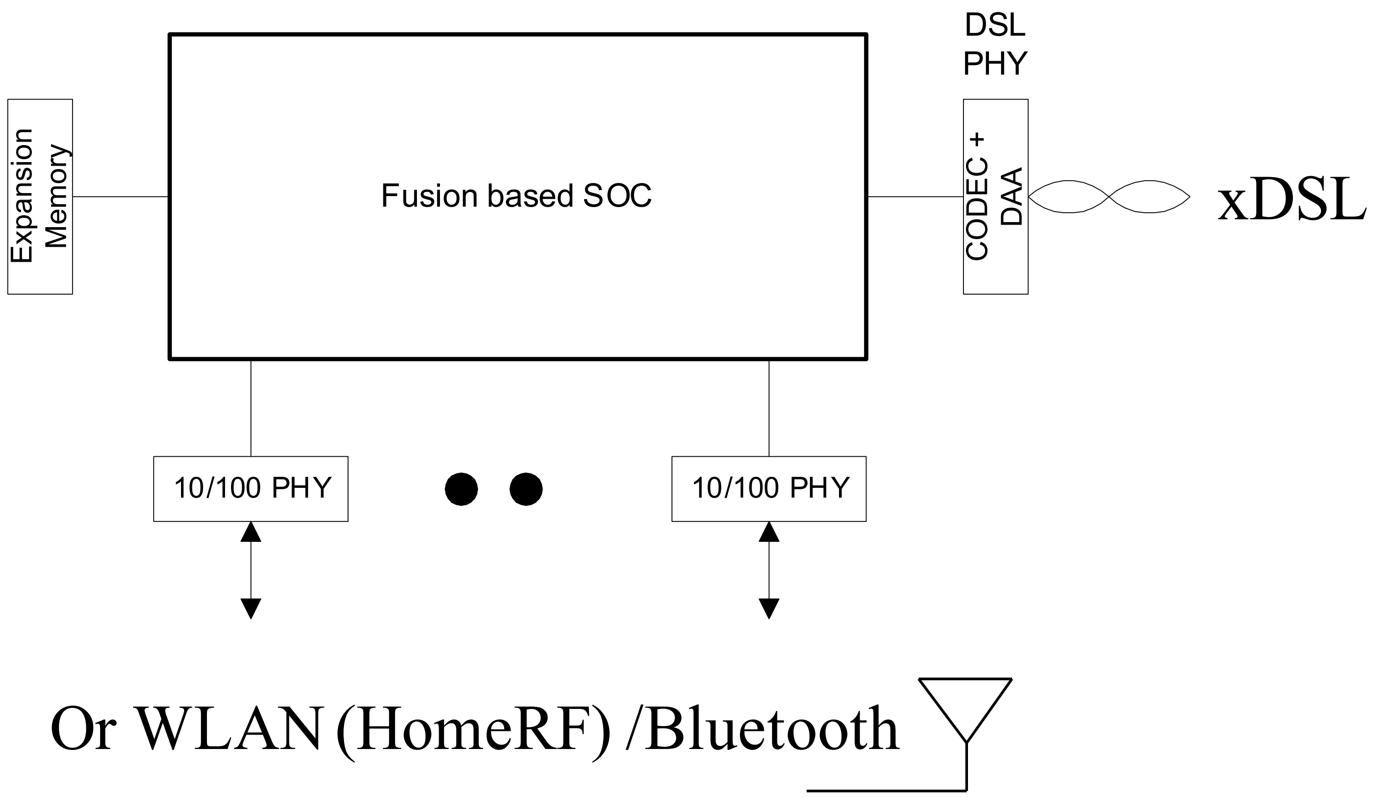
Matched filter uses dedicated hardware => SFA
Remainder of radio in software

Fusion Smart Cellphone Solution



Wired Application

Fusion Based SOHO Gateway/Router



Expansion Memory

Fusion based SOC

DSL PHY

CODEC + DAA

xDSL

10/100 PHY

● ●

10/100 PHY

Or WLAN (HomeRF) /Bluetooth

Software

- Unified hardware architecture leveraged to provide high productivity unified software development environment
  - Industry standard tools chain (such as Tornado)
  - MIPS based RISC ISA jumpstarts industry standard tools use.
- nBand core software competencies
  - DSP compiler extensions
    - Intrinsics/vector functions
    - Moving to full vectorizing compiler
  - Java support & runtime issues (“soft real-time” Java)
  - Key codec/algorithm development
- OS : Choice largely customer driven
  - Infrastructure => VxWorks, Handset => EPOC-32 & WinCE

Fusion Java

- Hardware interpreter
  - Converts to register based RISC instructions
  - Retain performance of hardware execution
  - Retain memory footprint advantages of direct bytecode execution
  - Avoid drawbacks of stack based machine
    - Leverage existing body of work for register based compilers
- Hardware + ISA support for
  - GC & Special OO functions
- Real-time focus!

Advisory Board

- Prof. Arogyaswami Paulraj, Stanford
  - Wireless systems design, low power wireless systems
    => access to labs at Stanford Center for Telecommunications
- Prof. David Patterson, U.C. Berkeley
  - Processor architecture, object oriented systems, IRAM
- Prof. Takayasu Sakurai, Tokyo U.
  - Embedded DRAM, low power VLSI design
- Dr. William Lee, Chief Scientist, Airtouch Communications
- Ron Ritchie, Ex. Computer Products, Ampex, Allied Signal, TI

Development Status

- First silicon - Cell Site Modem:
  - 4 lane, 450K gates, 2MB eDRAM, 10x10 .25micron, 200Mhz
- Logic design complete on:
  - MIPS-II processor and memory hierarchy
  - Vector DSP processor and memory hierarchy
- Tools - Functioning assembler, linker, loader, functional simulator/debugger, performance analyzer
  - Installed with:
    - Cisco broadband wireless group
    - Nortel and Motorola base station groups